Allowable Subject Matter

1. Claims 1-32, 37-40, 42-50, 53-86 and 93-97 are allowed over prior art.

The following is an examiner's statement of reasons for allowance: The prior art fail to teach or suggest with respect to claims 1-2, a switch fabric that includes a plurality of fabric gateways and an arbitration component configured to arbitrate a second plurality of RTSs, with respect to claim 3, wherein shifting the frame position for each cell of a column one additional row from a shifted frame position in a prior column, with respect to claim 5, shifted frame associated with a plurality of rows, each row associated with the shifted frame associated with an output link, respect to claims 7-10, reordering the plurality of cells within the frame to produce a shifted frame, each cell being reordered so that each row associated with the frame is uniquely associated with a time slot associated with the shifted frame, with respect to claim 11, time-division de-multiplexing a plurality of CTSs associated with a second frame, a first CTS from the plurality of CTSs associated with a second frame being associated with an availability of a first RTS associated with a cell from the plurality of cells of a first frame, with respect to claim 13, third frame cells being next in time from the plurality of cells associated with the first frame, with respect to claim 14, a cell slot translator configured to shift, with respect to claims 15-22 & 75, switch fabric that includes control portion that is unrelated to data portion of a cell, wherein the control portion includes RTS that identify virtual output queue (VOQ) having a buffered data portion, grouping a first plurality of RTSs and a second plurality of RTSs to produce a set of grouped RTSs, and arbitrating the set of grouped RTSs to produce a plurality of selected RTSs, with respect to claims 23-25, comparators coupled to a second memory wherein the comparators are configured to compare an input port schedule value with the plurality of input port requests to produce an output port grant, each comparator from the plurality of comparators

being further configured to compare an output port schedule value with a plurality of output port grants including the produced output port grant to produce an input port/output port designation, with respect to claims 26-27, a switch fabric that include grouping a plurality of RTS, forming a plurality of vectors based on the grouped RTSs, wherein each vector is associated with a timeslot representing a status of an output port request for each link, with respect to claims 28-32, RTSs being stored in a grouping memory and the arbitration component arbitrating concurrently the first plurality of RTSs to produce a plurality of selected RTSs, with respect to claims 37-40, data alignment controller configured to send a forwarding signal to the data storage controller at the latest receipt time associated with the plurality of data cells that is within a timeout period, with respect to claim 42, before sending plurality of cells, providing an idle cell for each cell from the plurality of cells that are not received within timeout period, with respect to claims 43-50, a first receipt time and a second data cell associated with the first time slot and a second receipt time later that the first receipt time, with respect to 53-64 and 71-73, a switching fabric that includes a plurality of fabric gateway components coupled to a plurality of multiplexer/de-multiplexer components and providing at least a third plurality of multiplexer/de-multiplexer components coupled to its own plurality of fabric gateway components, removably coupling the first plurality of switching components and the second plurality of switching components to the first plurality of multiplexer/de-multiplexer components, the second plurality of multiplexer/de-multiplexer components, with respect to claim 65, reconfiguring the first plurality of configurable components from the second configuration to the first configuration and removably coupling the second plurality of configurable components to the first plurality of configurable components, with respect to claims 62-64, a switch fabric that includes a plurality of fabric gateway components, a first set of configurable components coupled to a plurality of fabric gateway components, with respect to 69, providing at a third plurality of multiplexer/de-

multiplexer cards coupled to its own plurality of line cards, providing a second plurality of switching cards and removably coupling the first plurality of switching cards and the second plurality of switching cards to the first plurality of switching cards and the second plurality of switching cards to the first, second and third plurality of mux/demux cards, with respect to 74, distributed scheduler having a control path with a rate less than a rate of a control path of a centralized scheduler with a data path having a rate similar to the data rate of the distributed scheduler with respect to claims 76-82, buffering the plurality of cells in a plurality of virtual output queues (VOQ) wherein a first VOQ being associated with the first priority value and the second priority value, each remaining VOQ from the plurality of VOQs being uniquely associated with a remaining priority value from the plurality of priority values, with respect to claim 90, distributed scheduler specifies to a source the destination to which the source should forward data by providing a CTS to the source, with respect to claims 87, a scheduler arranged to receive control information and data from a source within a random time slots, and specify to source at least one destination to which the source should forward further data associated with the control data.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones
October 25, 2008

/Wing F. Chan/
Supervisory Patent Examiner, Art Unit 2619
10/27/08